Decommissioned IBM SP2

SP2 at the LRZ (1993-1998)

The SP2 at LRZ was comprised of 6 frames (racks) which contain 77 RS/6000 nodes. Used together, these 77 processors offer:

- 20.7 GFLOPS peak performance
- 16.7 GByte Memory
- 334 GByte disk
- approx. 14.6 GFLOPS LINPACK HPC-Performance

The SP2 has three types of nodes: Wide Nodes 67 MHz, Wide Nodes 77 MHz, and Thin Nodes 67 MHz.

The SP2 at LRZ has the following configurations:

<table>
<thead>
<tr>
<th>14 Wide Nodes</th>
<th>67 MHz POWER2 CPU</th>
<th>256 MByte Memory</th>
<th>256 KByte Data Cache</th>
<th>32 KByte Instruction Cache</th>
<th>256 Bit Memory-Bus</th>
<th>267 MFlOp/s Peak Performance</th>
<th>230 MFlOp/s Linpack HPC</th>
<th>2 SCSI-2 fast/wide Adapter</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Wide Nodes</td>
<td>77 MHz POWER2 CPU</td>
<td>1 GByte Memory (one node with 2 GByte)</td>
<td>256 KByte Data Cache</td>
<td>32 KByte Instruction Cache</td>
<td>256 Bit Memory-Bus</td>
<td>308 MFlOp/s Peak Performance</td>
<td>265 MFlOp/s Linpack HPC</td>
<td>2 SCSI-2 fast/wide Adapter</td>
</tr>
<tr>
<td>58 Thin-Nodes</td>
<td>67 MHz POWER2 CPU</td>
<td>128 MByte Memory</td>
<td>64 KByte Data Cache</td>
<td>32 KByte Instruction Cache</td>
<td>64 Bit Memory-Bus</td>
<td>267 MFlOp/s Peak Performance</td>
<td>180 MFlOp/s Linpack HPC</td>
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</table>

IBM's POWER Architectures

- In 1990, IBM announced the RISC System/6000 (RS/6000) family of superscalar workstations and servers
- POWER (Performance Optimized With Enhanced RISC) architecture
- An illustration of the processor's logical partitioning is provided here.
- RISC = Reduced Instruction Set Computer
- Superscalar = makes possible the simultaneous processing of multiple instructions. Includes:
  - Separate instruction cache (8 KB) and data cache (32 KB or 64 KB)
  - Combined floating point multiply-add instruction which allows a peak MFLOPS rate equal to two times the MHz rate while using a single functional unit.
  - Zero-cycle branches
  - Simultaneous running of fixed- and floating-point operations.
  - Overlapped running of register-register operations and load and store commands.
- 32 general purpose registers (32 bit)
- 32 floating point registers (64 bit - double precision)
- 128-bit memory addressing
- Different models depending upon clock rates, size of data cache, etc.
- Continued improvements in the POWER processor architecture have led to the POWER2 processor.